WHAT IS CLAIMED IS:

1. A processor comprising:

a first circuit configured to provide a first indication of whether or not at least one reservation is valid in the processor, wherein a reservation is established responsive to processing a load-linked instruction, wherein a load-linked instruction is a load instruction that is architecturally defined to establish the reservation, and wherein a valid reservation is indicative that one or more bytes indicated by the target address of the load-linked instruction have not been updated since the reservation was established; and

a second circuit coupled to receive the first indication;

wherein the second circuit is configured to select for issue, responsive to the first indication indicating no valid reservation, a speculative load-linked instruction; and

wherein the second circuit is configured not to select the speculative load-linked instruction for issue responsive to the first indication indicating the at least one valid reservation.

2. The processor as recited in claim 1 wherein the first circuit comprises a pipeline for processing load instructions, wherein the second circuit is configured not to select the speculative load-linked instruction if a load-linked instruction is in the pipeline, even if the first indication indicates no valid reservation.

3. The processor as recited in claim 1 wherein the first circuit includes a first storage device configured to store a target address of a load-linked instruction and a reservation

indication, wherein the reservation indication is indicative, in a first state, that a reservation is valid for the target address stored in the storage device and wherein the reservation indication is indicative, in a second state, that the reservation is not valid for the target address stored in the storage device.

4. The processor as recited in claim 3 wherein the first circuit is configured to store the target address in the first storage device responsive to the speculative load-linked instruction, and wherein the first circuit is further configured to place the reservation indication in the first state responsive to the speculative load-linked instruction.

5. The processor as recited in claim 4 wherein the first storage device is one of a plurality of storage devices, each configured to store a target address and a reservation indication.

6. The processor as recited in claim 5 further comprising a data cache including a plurality of banks, wherein each of the plurality of storage devices is associated with a different one of the plurality of banks.

7. The processor as recited in claim 6 wherein the first circuit is configured to store the target address of the speculative load-linked instruction into one of the plurality of storage devices corresponding to the one of the plurality of banks accessed by the speculative load-linked instruction, and wherein the first circuit is further configured to place the reservation indication in the one of the plurality of storage devices into the first state.

8. The processor as recited in claim 4 wherein the first circuit, in response to the speculative load-linked instruction not completing execution, is configured to place the reservation indication into the second state.

9. The processor as recited in claim 8 wherein the speculative load-linked instruction does not complete execution if the speculative load-linked instruction is replayed.

10. The processor as recited in claim 8 wherein the speculative load-linked instruction does not complete execution if a preceding branch instruction is redirected.

11. The processor as recited in claim 8 wherein the speculative load-linked instruction does not complete execution if the speculative load-linked instruction experiences an exception.

12. The processor as recited in claim 8 wherein the speculative load-linked instruction does not complete execution if a preceding instruction experiences an exception.

13. A method comprising:

determining whether or not at least one reservation is valid in a processor;

responsive to no valid reservation, selecting a speculative load-linked instruction for issue, wherein a reservation is established responsive to processing a load-linked instruction, and wherein a load-linked instruction is a load instruction that is architecturally defined to establish the reservation, and wherein a valid reservation is indicative that one or more bytes indicated by the target address of the load-linked instruction have not been updated since the reservation was established; and

responsive to at least one valid reservation, not selecting the speculative load-linked instruction for issue.

14. The method as recited in claim 13 further comprising not selecting the speculative load-linked instruction if a load-linked instruction is in a pipeline of the processor, even if the determining indicates no valid reservation.

15. The method as recited in claim 13 wherein the processor includes a first storage device configured to store a target address of a load-linked instruction and a reservation indication, wherein the reservation indication is indicative, in a first state, that a reservation is valid for the target address stored in the storage device and wherein the reservation indication is indicative, in a second state, that the reservation is not valid for the target address stored in the storage device, the method further comprising:

storing the target address in the first storage device responsive to the speculative load-linked instruction; and

placing the reservation indication in the first state responsive to the speculative load-linked instruction.

16. The method as recited in claim 15 wherein the first storage device is one of a plurality of storage devices, each configured to store a target address and a reservation indication, and wherein the processor includes a data cache including a plurality of banks, wherein each of the plurality of storage devices is associated with a different one of the plurality of banks, wherein the storing is performed to one of the plurality of storage devices responsive to which of the plurality of banks is accessed by the speculative load-linked instruction.

17. The method as recited in claim 15 further comprising, in response to the speculative load-linked instruction not completing execution, placing the reservation indication into the second state.

18. A carrier medium comprising one or more data structures representing a processor comprising:

a first circuit configured to provide a first indication of whether or not at least one reservation is valid in the processor, wherein a reservation is established responsive to processing a load-linked instruction, wherein a load-linked instruction is a load instruction that is architecturally defined to establish the reservation, and wherein a valid reservation is indicative that one or more bytes indicated by the target address of the load-linked instruction have not been updated since the reservation was established; and

a second circuit coupled to receive the first indication;

wherein the second circuit is configured to select for issue, responsive to the first indication indicating no valid reservation, a speculative load-linked instruction; and

wherein the second circuit is configured not to select the speculative load-linked instruction for issue responsive to the first indication indicating the at least one valid reservation.

19. The carrier medium as recited in claim 18 wherein the first circuit comprises a pipeline for processing load instructions, wherein the second circuit is configured not to select the speculative load-linked instruction if a load-linked instruction is in the pipeline, even if the first indication indicates no valid reservation.